REMARKS

Careful review and examination of the subject application are noted and appreciated.

Applicants thank Examiner Le for the indication of allowable matter.

INTERVIEW SUMMARY

Applicants' representative (John Ignatowski) spoke with Examiner Le via telephone on April 21, 2003 regarding the shallow reasoning for the §112 and §103 rejections in the February 27, 2003 final Office Action and §102 rejection in the August 28, 2002 original Office Action. Applicants' representative requested a new non-final Office Action with clear explanations why the claims were being rejected. The Examiner agreed to speak with his supervisor regarding the request. On May 8, 2003, The Examiner called Applicants' representative indicating that a supplemental final Office Action with expanded arguments would be issued with a new due date.

FINALITY OF THE OFFICE ACTION

Applicant's representative respectfully requests reconsideration of the finality of the May 21, 2003 Office Action. 37 CFR §1.104(b) states:

> (b) *Completeness of examiner's action.* The examiner's action will be complete as to all matters, except that in

> appropriate circumstances, such as misjoinder of invention, fundamental defects in the application, and the like, the action of the examiner may be limited to such matters of form need not be raised by the examiner until a claim is found allowable. (Emphasis added)

MPEP §706.07 further states:

> In making the final rejection, all outstanding ground of rejection of record should be carefully reviewed, and any such grounds relied on in the final rejection should be reiterated. They must also be clearly developed to such an extent that applicant may readily judge the advisability of an appeal unless a single previous Office action contains a complete statement supporting the rejection. (Emphasis added)

The Office Action has failed to clearly developed the rejections for independent claims 18 and 20. In particular, page 3, lines 12-13 of the Office Action state that claims 18 and 20 are rejected under 35 USC §103(a). However, the subsequent text of the Office Action provides no rational or explanation for the rejection. As such, the final rejections are premature and should be withdrawn. Applicants' representative again requests that a non-final Office Action be provided to allow a reasonable opportunity to respond absent the restrictions of after-final practices.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found in claims 2 and 12. Thus, no new matter has been added and no new issues have been raised.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1, 3, 4, 10, 11, 13 and 14 under 35 U.S.C. §102(e) as being anticipated by Lien '651 has been obviated by appropriate amendment and should be withdrawn.

Lien discloses a high voltage tolerable input buffer. In contrast, the present invention provides an apparatus generally comprising a first device and a first resistive element. The first device generally comprises (i) a first gate configured to receive an input voltage ranging from up to twice a first supply voltage with respect to a second supply voltage to at least the second supply voltage, (ii) a first drain configured to receive the first supply voltage, and (iii) a first source coupled to a first output. The first resistive element may have (i) a first side coupled to the first source and (ii) a second side configured to receive the second supply voltage, wherein the apparatus is arranged such that a maximum voltage drop across a gate oxide of the first device does not exceed a difference between the first supply voltage and the second supply voltage.

Claim 1 provides a first device comprising (i) a first gate configured to receive an input voltage ranging from up to twice a first supply voltage with respect to a second supply voltage to at least the second supply voltage, wherein the apparatus is arranged such that a maximum voltage drop across a gate oxide of the first device does not exceed a difference between

the first supply voltage and the second supply voltage. Lien appears to be silent and the Office Action has not provided any evidence that the voltage across the gate oxide of a transistor 501 in FIG. 7 of Lien will not exceed a difference between supply voltages Vcc and Vss when Vin=2*(Vcc-Vss). The arguments on page 4, lines 8-14 of the Office Action regarding an input voltage of twice the supply voltage do not address the claim language and thus are moot. In particular, the language moved from claim 2 into claim 1 does not place any limitations on the gate oxide thickness or threshold voltage. Thus, assertions that modifications to the gate oxide thickness or threshold voltage of the transistor would be obvious to an engineer are irrelevant. Therefore, Lien does not appear to disclose or suggest a first device comprising (i) a first gate configured to receive an input voltage ranging from up to twice a first supply voltage with respect to a second supply voltage to at least the second supply voltage, wherein the apparatus is arranged such that a maximum voltage drop across a gate oxide of the first device does not exceed a difference between the first supply voltage and the second supply voltage as presently claimed. Claim 11 provides language similar to claim 1. As such, claims 1 and 11 are fully patentable over the cited reference and the rejection should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 2, 5, 7-9, 15-18 and 20 under 35 U.S.C. §103(a) as being unpatentable over Lien in view of Ito et al. '247 (hereafter Ito) is respectfully traversed and should be withdrawn.

Claim 5 provides a first device comprising a native NMOS device. Page 4, lines 8-14 of the Office Action state that native MOS transistors are well known in the art and thus it would have been obvious for an engineer to modify Lien with a native MOS transistor. However, the Office Action fails to provide any motivation to replace the transistor 501 of Lien with a native MOS transistor. The fact that references can be combined or modified is not sufficient to establish *prima facie* obviousness (See MPEP §2143.01). Furthermore, Ito appears to be silent on using native MOS transistors. Therefore, the Office Action has failed to establish *prima facie* obviousness for modifying Lien to produce a first device comprising a native NMOS device as presently claimed. Claims 8, 16 and 17 provide language similar to claim 5. As such, claims 5, 8, 16 and 17 are fully patentable over the cited references and the rejection should be withdrawn.

Claim 18 provides a first stage having an output and a second stage having a second resistive element and coupled to the output of the first stage. In contrast, Lien appears to be silent regarding a second stage coupled to the output of a first stage,

Only FIG. 3 of Ito shows two stages coupled in series. However, the block 31 in FIG. 3 of Ito is silent regarding a second resistive element. Furthermore, the Office Action has not provided any rational, explanation, evidence or motivation that an obvious combination of Lien and Ito would somehow teach or suggest the claim language. Therefore, Lien and Ito alone, or in combination, do not appear to teach or suggest a first stage having an output and a second stage having a second resistive element and coupled to the output of the first stage as presently claimed. As such, claim 18 is fully patentable over the cited references and the rejection should be withdrawn.

Claim 20 provides (i) a first stage receiving an input voltage and having an output and (ii) a second stage receiving the input voltage and coupled to the output. In contrast, both Lien and Ito appear to be silent regarding a first stage and a second stage receiving the same input voltage and being coupled to the same output. Furthermore, the Office Action has not provided any rational, explanation, evidence or motivation that an obvious combination of Lien and Ito would somehow teach or suggest the claim language. Therefore, Lien and Ito alone, or in combination, do not appear to teach or suggest (i) a first stage receiving an input voltage and having an output and (ii) a second stage receiving the input voltage and coupled to the output as presently

claimed. As such, claim 18 is fully patentable over the cited references and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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